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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PATEL, PARESH H	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 11/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,683	UCHIDA, REN	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Hideaki (JP 2000-165244).

Regarding claim 9, Hideaki in fig. 1-4 discloses: a testing device for semiconductor integrated circuits, comprising:

a semiconductor integrated circuit [LCD IC, see Abstract] integrated with a plurality of base power supply input terminals [11 and paragraph 0001], a base voltage generation circuit [using 12] having a Gamma correction resistance [12], and

a plurality of D/A converters [DAC], generating gradation output voltage characteristics [no shown, inherent at output of output terminal (1-N) of 6]; and

a comparison judgment circuit [test equipment of paragraph 0004] for comparing gradation output voltages and reference voltages, for a plurality of gradation output voltages in parallel simultaneously [paragraph 0004].

Regarding claim 10, Hideaki in fig. 1-4 discloses a testing method for semiconductor integrated circuits comprising:

setting of an upper limit level [5V] and lower limit level [0V] of graduation output voltage level intervals [intervals shown in fig. 1 at 5] in between base power supply terminals being test objects;

second step of setting a test generation number [depend on total no of 11] and a gradation output voltage expectation value level for a graduation output voltage level [i.e. 0.5V or less];

sequentially testing [using 13 and 14 between each 11] all graduation output voltage levels in between base power supply terminals for each graduation level [paragraphs 0019-0020];

judging [last two lines of paragraph 0019] whether a test result at a graduation output voltage level is a failure, and if so ending the test; and

repeating the second step of setting, sequentially testing and judging until a designated gradation level or test failure [for every terminal 11 using 13 and 14].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art in view of Tamai et al. (JP 09-068692).

Regarding claim 1, Applicant admitted prior art (hereinafter APA) in fig. 1-6 discloses: a testing method for semiconductor integrated circuits wherein,

in the testing method testing by a semiconductor testing apparatus having a comparison judgment circuit [60 or 70 or 7] judging a semiconductor integrated circuit [1 or 51 or 81] integrated with a plurality of DA converters [2-1 to 2-m] and a base voltage generation circuit [8] determining the gradation output voltage characteristics, by comparison of the gradation output voltages and reference voltages [see Analog Gradation voltage curve], wherein **the gradation level intervals to be the test objects** [e.g. interval of 2-1, 2-2 and 2-3 of fig. 1] are decided by the setting of different voltages [V1-V6] to be applied at the base power supply input terminals [terminals of 1 where V1-V6 applied] of said base voltage generation circuit [8]; and

said voltages are supplied at and between said base power supply input terminals from said semiconductor testing apparatus [7, terminals of 1 for V1-V6]; and

by assigning correspondence between the input gradation data signals [signal from 6-1 to 6-x] of the gradation levels of that interval, and the gradation output voltages [output of 3-1 to 3-m], the gradation output voltage testing through said semiconductor testing apparatus is made to be digital judgment [using 60].

APA lacks assigning correspondence between the input gradation data signals [signal from 6-1 to 6-x] of the **gradation levels of that interval**, and the gradation output voltages [output of 3-1 to 3-m]. Tamai et al. (hereafter Tamai) discloses assigning correspondence between the input gradation data signals [see fig. 13] of the **gradation levels of that interval** [fig. 4, fig. 13 and paragraph 0005 and 0012], and the

gradation output voltages [see fig. 13]. It would have been obvious to one having ordinary skill in the art to test liquid crystal driver at that interval, in order to reduce size of driver and current consumption without using a complex circuit structure.

Regarding claim 2, APA in fig. 3-4 discloses: a testing method for semiconductor integrated circuits according to claim 1, wherein, according to the voltages provided at and between the base power supply input terminals from said semiconductor testing apparatus, said base voltage generation circuit increases or decreases the neighboring gradation output potential differences of every analog voltage output of said semiconductor integrated circuit [Gradation voltage of fig. 3 and 4 at output 3-1 to 3-m for Digital Judgment Comparator using Decoder 82].

Regarding claim 3, APA discloses: a testing method for semiconductor integrated circuits according to claim 1, wherein, by assigning correspondence between the voltage settings provided from said semiconductor testing apparatus and the input data, said DA converters and the base voltage generation circuit selectively test the output levels of the analog voltage outputs [fig. 4].

Regarding claim 4, APA discloses: a testing method for semiconductor integrated circuits according to claim 1, wherein, proving of the reliability of the test accuracy is made possible by treating the mutual relationship between the computation of the input data corresponding to every output voltage level and of the expectation values of the output voltages in the semiconductor integrated circuit specification and the setting of the output voltage expectation value levels, and the voltage judgment value levels of said comparison judgment circuit carrying out the judgment of the output

voltages, and the change of the setting of the test numbers with time, altogether as address or parameter management [using 64 and fig. 6].

Regarding claim 5, APA discloses: a testing device [60, 70, 51] for semiconductor integrated circuits [51, 81], wherein, in a judging testing apparatus [60, 70], through a comparison judgment circuit [51], a semiconductor integrated circuit integrated with a plurality of DA converters [2-1 to 2-m] and a base voltage generation circuit [8] determining the gradation output voltage characteristics, by comparison of said gradation output voltages and reference voltages[see Analog Gradation voltage curve],

APA lacks different voltages are output to the base power supply input terminal for the end of one side of the gradation level interval being the test object of said semiconductor integrated circuit, and the base power supply input terminal of the other end of said interval. Tamai in fig. 4 discloses different voltages are output to the base power supply input terminal for the end of one side of the gradation level interval being the test object of said semiconductor integrated circuit, and the base power supply input terminal of the other end of said interval. It would have been obvious to one having ordinary skill in the art to test liquid crystal driver (or IC) at that interval, in order to reduce size of driver and current consumption without using a complex circuit structure.

Regarding claim 6, Tamai in fig. 4 discloses: a testing device for semiconductor integrated circuits according to claim 5, wherein, said voltages are output to more than two base power supply input terminals including the base power supply input terminal at

the end of at least one side of the gradation level interval being the test object of the semiconductor integrated circuits.

Regarding claim 7, Tamai in fig. 4 discloses: a testing device for semiconductor integrated circuits according to claim 5, wherein, base power supply input terminals not connected with the semiconductor testing apparatus are disposed in the gradation level interval being the test object of the semiconductor integrated circuit [terminal of AS1-AS8].

Regarding claim 8, Tamai in fig. 14 discloses: a testing device for semiconductor integrated circuits according to claim 5, wherein, more than two gradation level intervals being the test objects of the semiconductor integrated circuits are disposed [using ASW1 and ASW2].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 703-306-5859. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Paresh Patel
Nov. 14, 2003